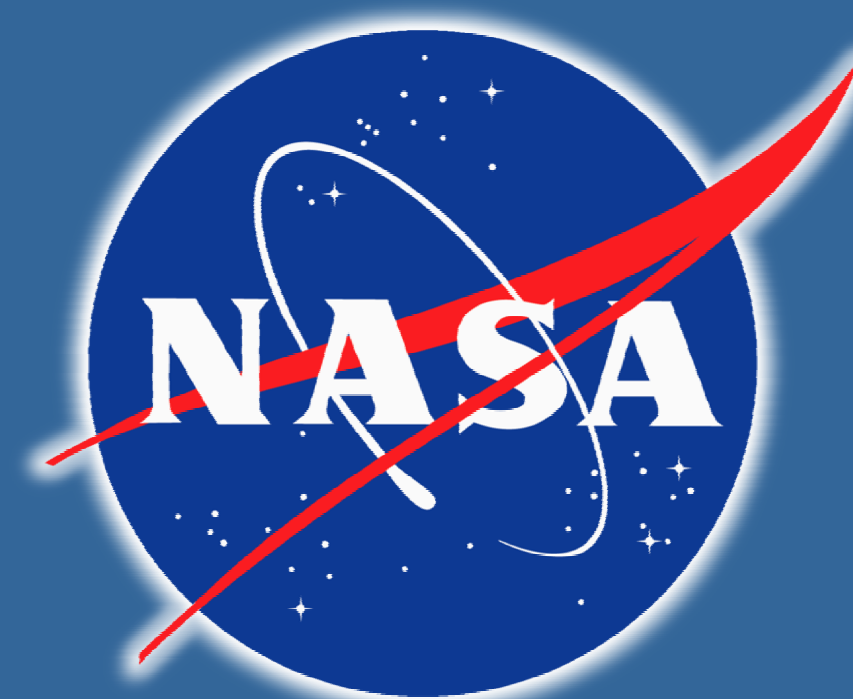




# Failure Analysis for Electronics

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## Overview

	Failure Modes	Failure Analysis Techniques
External and Package Failure	Package mechanical damage	OM, SLAM, SAM
	Corrosion, contamination	OM, ESEM, SEM, EDX, SLAM
	Plastic cracking	SAM, IRM, ESEM, SEM, OM
	Plastic/die delamination	SAM, IRM, SLAM
Internal Failure	Electrical overstress	MP, LCD, IRM, OM, ESEM
	Electrostatic discharging	OM, ESEM, SEM
	Electromigration	XM, SAM
	Die-attach voiding	SAM, SLAM
	Die-attach delamination	OM, SLEM, ESEM, EDS, SLAM, SAM
	Corrosion, contamination	SAM
	Interfacial delamination	SAM, ESEM
	Die cracking	SAM, SLAM
	Metallization microcracking	ESEM, SEM, SAM
	Oxide breakdown	EM, ESEM, SEM
	Si or Ga-As defect	TEM, ESEM, SEM

OM – Optical Microscopy  
SLAM – Scanning laser acoustic microscopy  
SAM – Scanning acoustic microscopy  
ESEM – Environmental scanning electron microscopy  
SEM – Scanning electron microscopy  
EDX – Energy-dispersive X-ray spectroscopy  
IRM – Infrared microscopy  
TEM – Transmission electron microscopy  
XM – X-Ray microscopy

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## Motivation

- For several electronic components exact failure mechanisms are not yet known
- Systematic identification will be useful in determining the underlying physical failure mechanisms, which can ultimately lead to pinpointing the failures' root causes and aid in developing physics-of-failure models for prognostics

## Suggested Approach

- Failure analysis will involve:
  - Verification that failure occurred
  - Determination of failure mode (symptom)
  - Determination of failure mechanism and root cause
  - Suggest corrective/preventive action
- Techniques like optical and scanning electron microscopy are expected to reveal interesting features

## Failure Mechanisms

### Failure mechanisms for power transistors

- Intrinsic faults related to transistor physics
  - Dielectric breakdown
  - Hot carrier injection
  - Electromigration
- Extrinsic faults related to transistor packaging
  - Contact migration
  - Wire lift
  - Die solder degradation
  - Package delamination

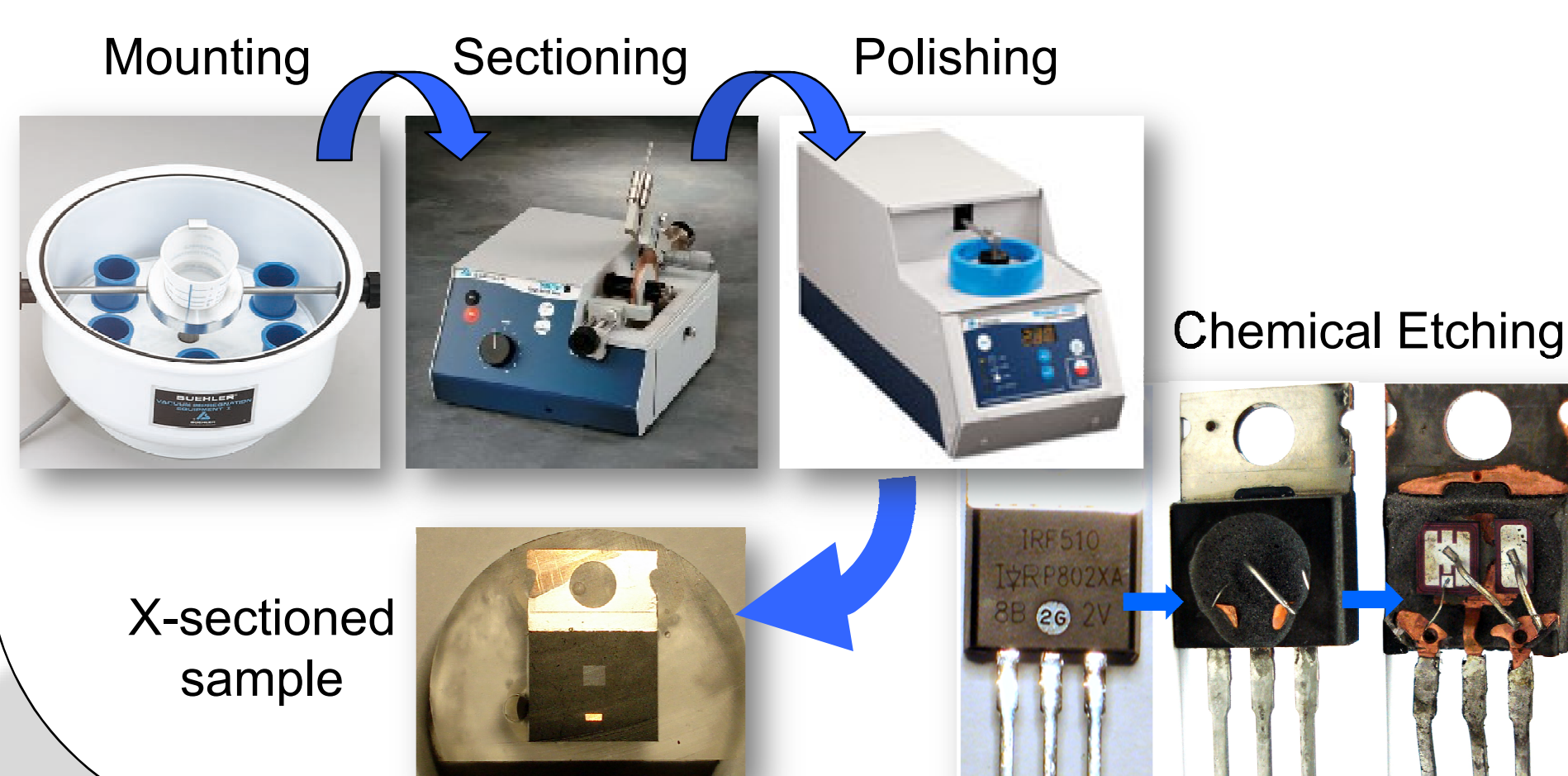
### Aging under thermal and electrical stress

- Thermal stress
  - Thermal cycling
  - Chronic temperature overstress
- Electrical stress
  - Electrostatic discharge
  - Inductive switching
  - Electromagnetic pulses
  - Chronic over-voltage and over-current

## Methodology

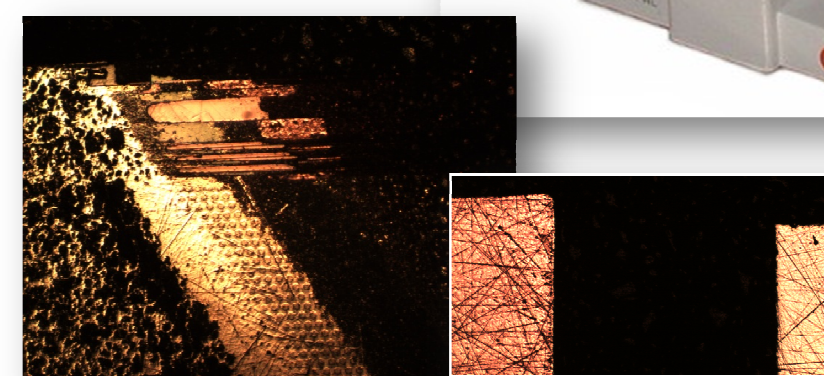
### Sample Preparation

- Outer packages must be removed to reveal internal structure of the devices
- De-capsulation of plastic packages
  - Expose die and interconnects for failure analysis
  - There are three methods
    - Mechanical de-capsulation (saw/sanding)
    - Plasma etching
    - Chemical de-capsulation (manual or automated)

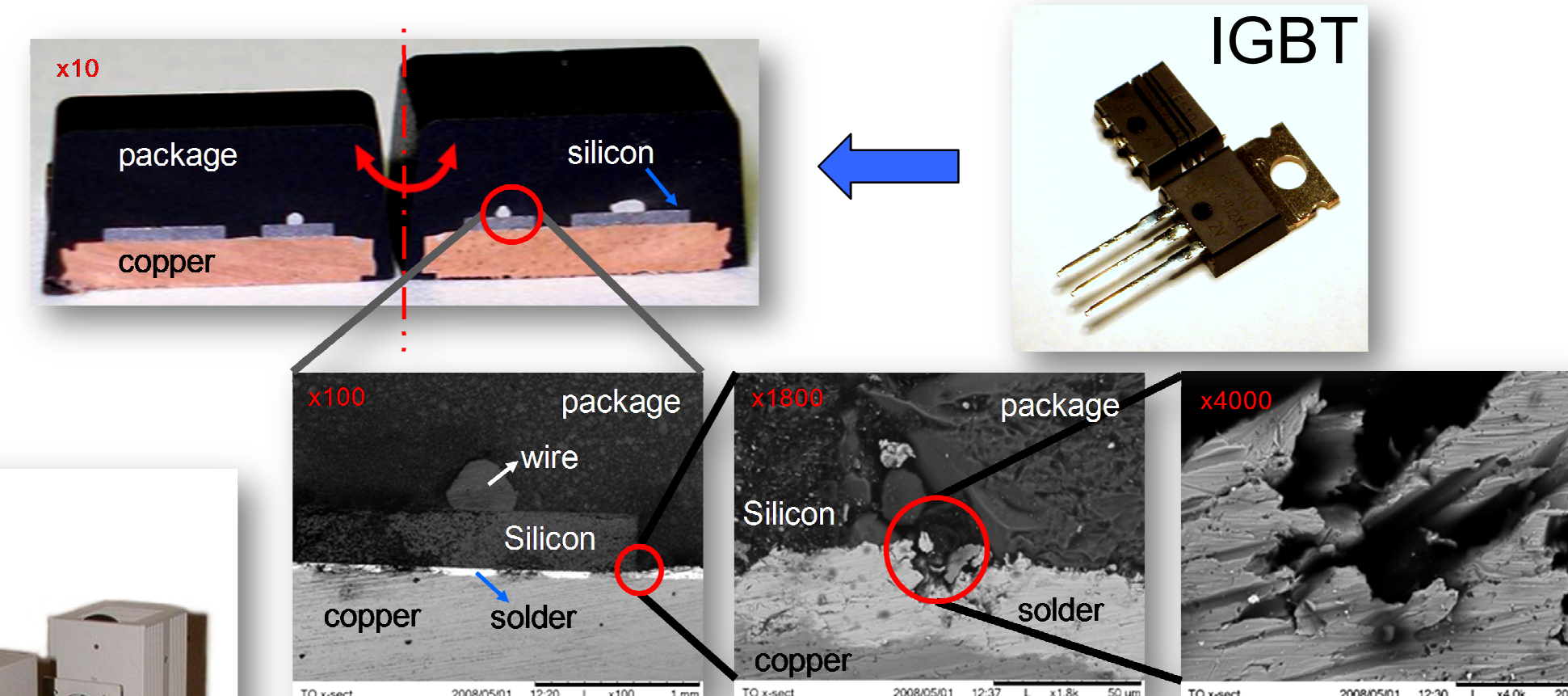


### Optical Microscopy

- Employed after sample preparation for external inspection and to assess degradation and locate/identify root causes of failures
- Illumination arrangements:
  - Bright field (most common, for opaque samples)
  - Dark field (accentuates surface irregularities)
  - Polarized light (for locating interfaces and examining grain structure of metals)
  - Differential interference contrast (allows visualization of minute elevation differences in surface)
  - Fluorescence (for contamination identification and to detect foreign materials)



### Electron Microscopy



- Can provide materials and micro-structural information such as grain, size distribution, surface roughness and porosity, particle size, materials homogeneity and inter-metallic distribution
- Can be used in failure analysis to
  - Find location of contamination and mechanical damage
  - Provide evidence of ESD
  - Detect micro-cracks

## Results

### Experiments on IGBT

- A preliminary thermal overstress aging test was conducted on IGBTs
- International Rectifier IRG4BC30KD with 600V/15A rating in a T0220 package
- The temperature was measured from the IGBT package without external heat
- The experiment was stopped after thermal runaway or latch-up failure
- A hysteresis temperature controller was used to control the aging process switching the gate voltage
- Aging experiment settings:
  - Serial resistive load of 0.2 Ohms
  - Gate driven by a PWM signal at 10V, 10KHz and 40% duty cycle
  - Power supply at 4V on load circuit
  - Temperature thresholds: Low=329°C, High=330°C, and Runaway= 340°C

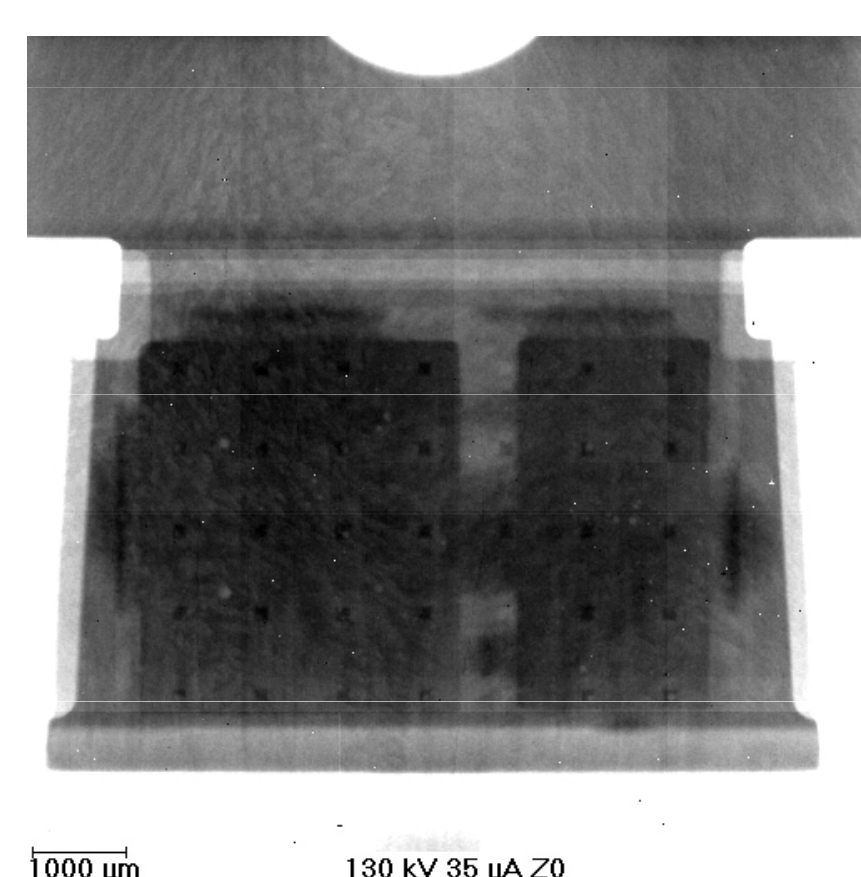
### Approach

Perform failure analysis for pristine and aged devices in order to identify the damage generated by the thermal overstress and identify the failure mechanisms triggered by the aging.

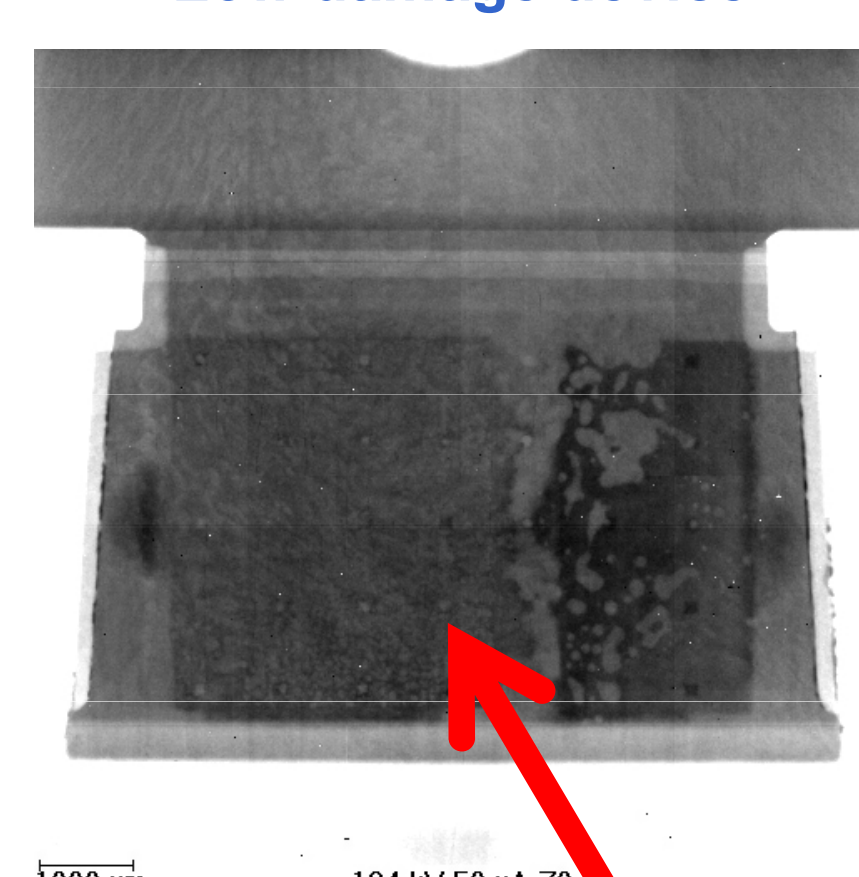
### X-Ray Analysis

- Failure analysis by x-ray imaging shows the presence of voids in the die attach area
- Failure mechanism triggered by the thermal overstress aging seems to be die attach degradation

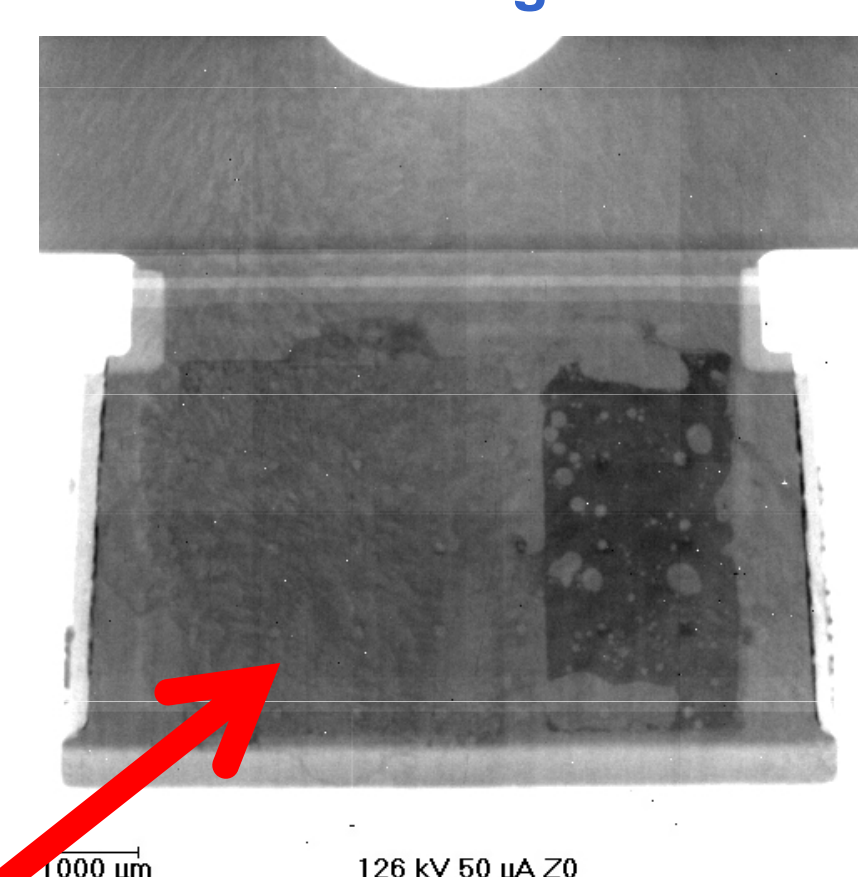
Pristine device



Low damage device



Medium damage device



Die attach damage